• Features

- Used with the DC003 and DC004 circuits to implement a program control device interface.
- Used with the DC003, DC004, DC006, and DC010 circuits to implement a direct memory access interface.
- Functions as a bidirectional buffer between the device logic and computer bus.
- Includes comparison circuit for device address selection.
- Includes constant generator for interrupt vector address generation.
- Includes Q-bus drivers and receivers.

• Description

The DC005 4-bit transceiver, contained in a 20-pin dual-inline package (DIP), implements low-power Schottky technology and functions as a bidirectional buffer between a data bus and peripheral device logic bus. It includes a comparison circuit for device address selection and a constant generator for interrupt-vector address generation. It provides high-impedance inputs and high-drive, open-collector outputs to allow direct connection to a computer data bus structure. The bidirectional device port includes TTL inputs and three-state driver outputs. Figure 1 is a simplified logic diagram of the DC005.

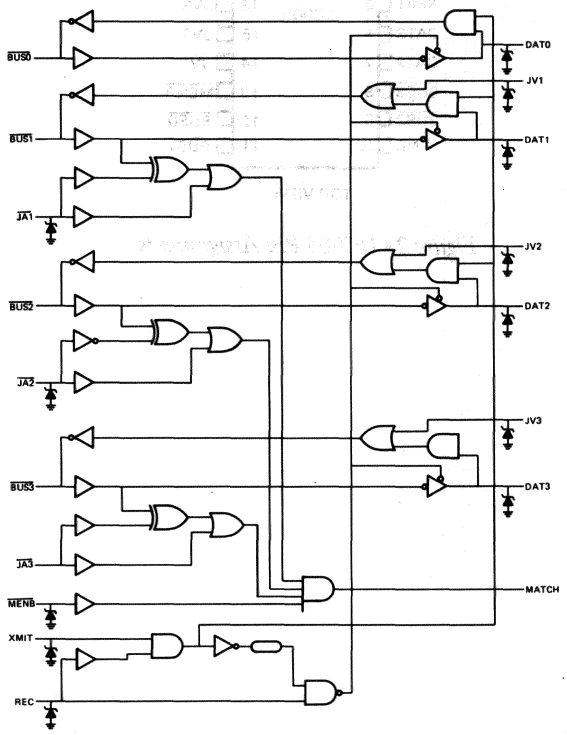

Figure 1 • DC005 Simplified Logic Diagram

Three address select inputs can be configured by jumper leads to enable a comparison to be made between the jumper connections and three bus inputs. An open-collector MATCH output allows several transceiver outputs to be gated to form a composite address match signal. The address jumpers can also be configured to disable the address match condition. The address match condition is controlled by an input line that can enable or disable the MATCH output.

Three vector inputs can also be configured by jumper leads to generate a constant vector value that is transferred to the computer bus. The vector inputs directly drive three of the bus lines to override the function of the control lines.

Two control signals are decoded to select the receive data and transmit data operation and to disable the operation of the device.

▪ Pin and Signal Descriptions

This section provides a brief description of the input and output signals and power and ground connections of the DC005 20-pin DIP. The pin assignments are identified in Figure 2 and the summarized in Table 1.

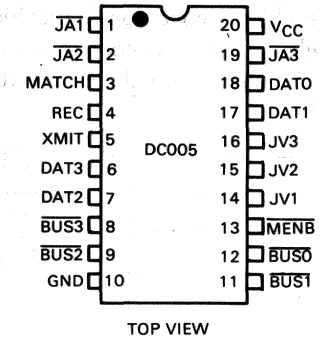

Figure 2 ▪ DC005 Pin Assignments

Table 1 • DC005 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
8-12	$\overline{BUS<3:0>}$	input[1]/output[2]	Bus 3-0 lines—These lines are bidirectional and connect to the BDAL lines of the Q-bus. A low is equal to 1.
6,7,17,18	DAT<3:0>	inputs/outputs[3]	Data 3-0 lines—These lines transfer the inverted data from the bus to the device in receive mode and from the device to the bus in transmit mode. During disable mode, the outputs are at a high impedance.
16-14	JV<3:1>	inputs[4]	Vector jumpers 3-1—These lines directly drive the $\overline{BUS<3:1>}$ lines. A ground connection or an open jumper pin causes an open condition on the corresponding bus pin if the $\overline{XMIT}$ signal is asserted. A high (5 V) connection to the jumper pin will cause a one (low) on the corresponding bus pin. The $\overline{BUS<0>}$ line is not controlled by a jumper.
13	$\overline{MENB}$	input[1]	Match enable—A low input will enable the MATCH output when a match occurs between the level of $\overline{BUS<3:1>}$ signals and the address jumpers JA3 through JA1.
3	MATCH	output[2]	Address match—This output is open when a match occurs between the level of the $\overline{BUS<3:1>}$ lines and the levels selected by the address jumpers JV3 through JV1. The output is low when no match occurs.
19,2,1	$\overline{JA<3:1>}$	inputs[5]	Address jumpers—When connected to ground, these pins allow a match to occur with a one (low) on the corresponding $\overline{BUS<3:1>}$ lines. When these lines are not connected, a match can occur with a zero (high) level on the corresponding bus lines. When connected to 5 V, the corresponding address bit is disconnected.
5 4	XMIT REC	inputs[3]	Transmit/Receive control—Controls the operation of the transceiver as follows: REC XMIT Function 0 0 Disable(open): BUS and DAT lines 0 1 Transmit: DAT to BUS lines 1 0 Receive: BUS to DAT lines 1 1 Receive: BUS to DAT lines
20	V_{cc}	input	Voltage—Power supply dc voltage
10	GND	input	Ground—Common ground reference

[1]high-impedence
[2]open-collector
[3]TTL level
[4]TTL level with pull-down circuit
[5]three-state

• Application Information

Refer to the *Chipkit Users Manual LSI-11 Bus Interface Chips* (document no. EJ-01387-92) for general application information. The Q-bus is an LSI-11 bus.

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the DC005 are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Operating temperature (T_A): 0°C to 70°C
- Supply voltage (V_{CC}): 5.0 V ±5%

Mechanical Configuration

The physical dimensions of the DC005 20-pin DIP are contained in Appendix E. The materials and construction of the molded DIP are defined in Digital Specification A-PS-2100002-GS.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Supply voltage (V_{CC}): 7.0 V
- Input voltage (V_I): 5.5 V
- Operating temperature (T_A): 0°C to 70°C (32°F to 158°F)
- Storage temperature (T_S): –65°C to 150°C (–149°F to 302°F)

Recommended Operating Conditions

- Supply voltage (V_{CC}): 4.75 V (minimum), 5.0 V (normal), 5.25 V (maximum)
- Supply current (I_{CC}): 120 mA (maximum)
- Free-air temperature: 0°C to 70°C (32°F to 158°F)
- Relative humidity: 10% to 95% (noncondensing)

dc Electrical Characteristics

The dc electrical characteristics of the DC005 for the operating voltage and temperature ranges specified are listed in Tables 2 through 6. Table 2 lists the dc specifications for the TTL input and outputs that do not connect to the bus. Table 3 lists the dc specifications for the high-impedance receiver inputs from the bus. Table 4 lists the dc specifications for the open-collector driver outputs that connect to the bus. Table 5 lists the dc specifications for the three-state jumper lead connections inputs used for the address comparison logic. Table 6 lists the dc specifications for the TTL jumper leads connections used to select a vector address. Refer to Appendix C for test circuit configurations listed in the tables.

Table 2 • DC005 TTL Input and Output Parameters (nonbus)

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}		2.0	—	V	C1,C2
Low-level input voltage	V_{IL}		—	0.8	V	C1,C2
Input clamp voltage	V_I	V_{CC}=4.75 V I_I=−18 mA	—	−1.2	V	C3
High-level output voltage	V_{OH}	V_{CC}=4.7 V I_O=−1.0 mA	3.65	—	V	C1
Low-level output voltage	V_{OL}	V_{CC}=4.75 V I_O=20 mA	—	0.5	V	C2
Input current at maximum input voltage	I_I	V_{CC}=5.25 V V_I=5.5 V	—	1.0	mA	C4
High-level input current	I_{IH}	V_{CC}=5.25 V V_I=2.7 V				C4
		Receive:	—	100	μA	
		Transmit:	—	50	μA	
Low-level input current	I_{IL}	V_{CC}=5.25 V V_I=0.5 V				C5
		Receive:	—	−2.2	mA	
		Transmit:	—	−1.1	mA	
Short-circuit output current	I_{OS}	V_{CC}=5.25 V[1]	−40	−100	mA	C6
Supply current	I_{CC}	V_{CC}=5.25 V	—	120	mA	C7
High-impedance state output current[2]	I_O	V_{CC}=5.25 V				
		V_I=3.65 V	—	100	μA	
		V_I=0.5 V	—	−0.36	mA	

[1]Not more than one output shall be short circuited at a time and the duration of the short shall not exceed 1 second.

[2]Off state, DAT<3:0> pins only.

Table 3 • DC005 High-impedance Bus Receiver Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}	$V_{CC}=4.75$ V	1.53	—	V	C1,C2
		$V_{CC}=5.25$ V	1.70	—	V	
Low-level input voltage	V_{IL}	$V_{CC}=4.75$ V	—	1.30	V	C1,C2
		$V_{CC}=5.25$ V	—	1.47	V	
Input clamp voltage	V_I	$I_I=-18$ mA, $V_{CC}=4.75$ V	—	-1.2	V	C3
High-level input current	I_{IH}*	$V_I=3.8$ V [2]				C4
$\overline{\text{MENB}}$		$V_{CC}=0$ V	—	40	μA	
		$V_{CC}=5.25$ V	—	40	μA	
$\overline{\text{BUS}}$		$V_{CC}=0$ V	—	65	μA	
		$V_{CC}=5.5$ V	—	65	μA	
Low-level input current	I_{IL}	$V_I=0.5$ V				C5
		$V_{CC}=0$ V	—	-10	μA	
		$V_{CC}=5.25$ V	—	-10	μA	

*Includes open-collector leakage current on bus

Table 4 • DC005 Open-collector Bus Driver Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
Output reverse current*	I_{OH}	$V_{CC}=4.75$ V, $V_{OH}=5.25$ V	—	25	μA	C1
Low-level output voltage	V_{OL}	$V_{CC}=4.75$ V				C2
MATCH		$I_{sink}=8$ mA	—	0.5	V	
$\overline{\text{BUS<3:0>}}$		$I_{sink}=70$ mA	—	0.8	V	
		$I_{sink}=16$ mA	—	0.5	V	

*Pin 3 only (MATCH). For BUS<3:0> pins, refer to I_{IH} Table 2.

Table 5 • DC005 TTL Three-state Address Input Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}		4.75	—	V	C1
Low-level input voltage	V_{IL}		—	0.3	V	C1
Open-circuit input voltage	V_{OP}	4.75 <V_{CC}> 5.25	1	2	V	

Table 6 • DC005 TTL Vector Input Parameters

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}		2.0	—	V	C1
Low-level input voltage	V_{IL}		—	0.8	V	C1
Input clamp voltage	V_I	V_{CC}=4.75 V I_I=−18 mA	—	−1.2	V	C3
High-level input current	I_{IH}	V_{CC}=5.25 V V_I=2.4 V	—	1.2	V	C4
Low-level input voltage forcing current	V_{II}	V_{CC}=4.75 V I_I=0.1 mA	—	0.8	V	C4*
Input current at maximum input voltage	I_{IL}	V_{CC}=5 V V_I=0.4 V	50	200	μA	C5

*Remaining inputs open.

ac Electrical Characteristics

The input and output signal timing parameters for the DC005 are grouped by functions and shown in Figure 3. Figure 4 shows the load circuits used to measure the signal timing for the open-collector and three-state outputs. Figure 5 shows the three-state voltage waveform parameters. Refer to Appendix D for the standard input and output voltage waveforms parameters used to measure propagation delay.

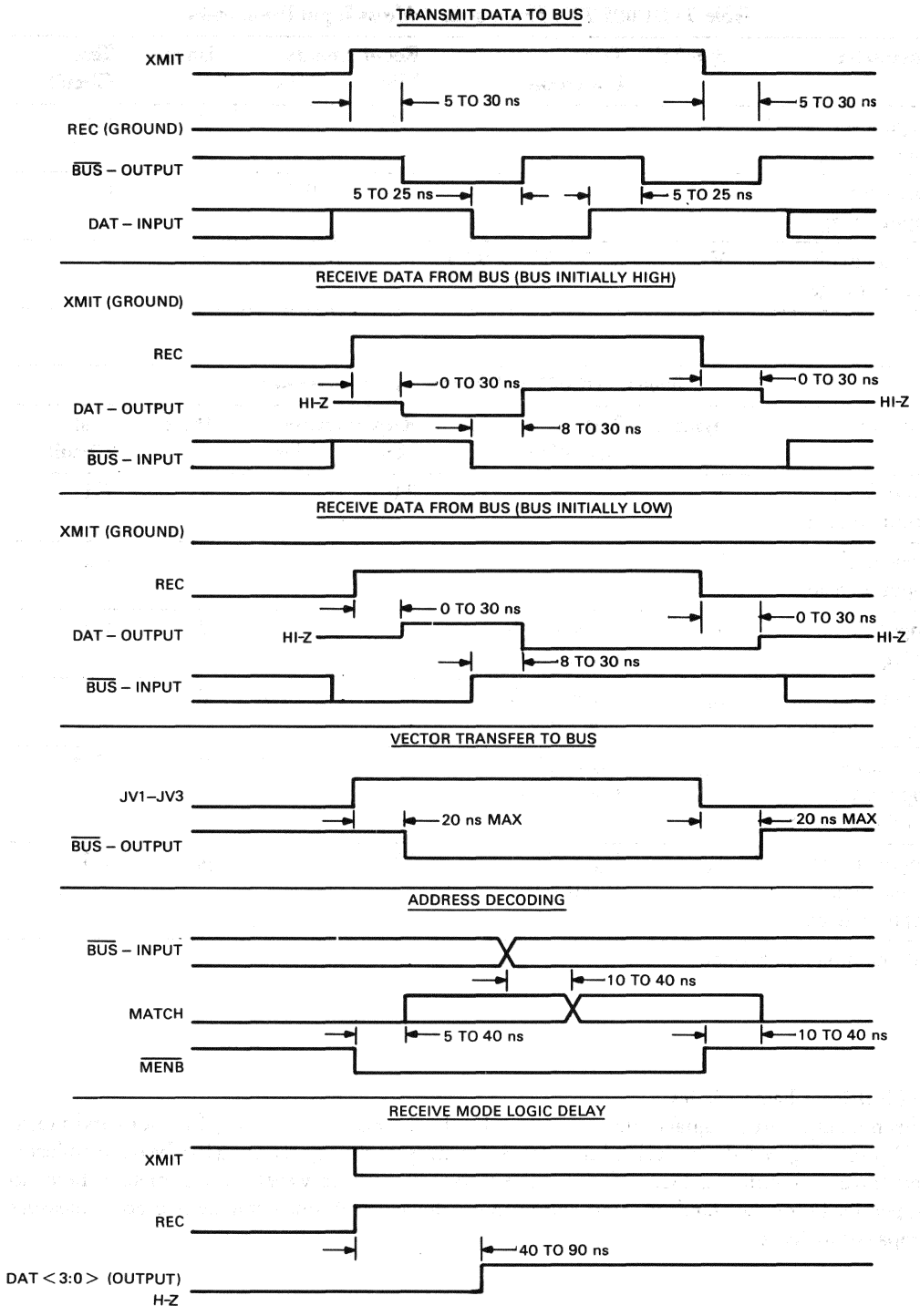

Figure 3 • DC005 Signal Timing Sequence

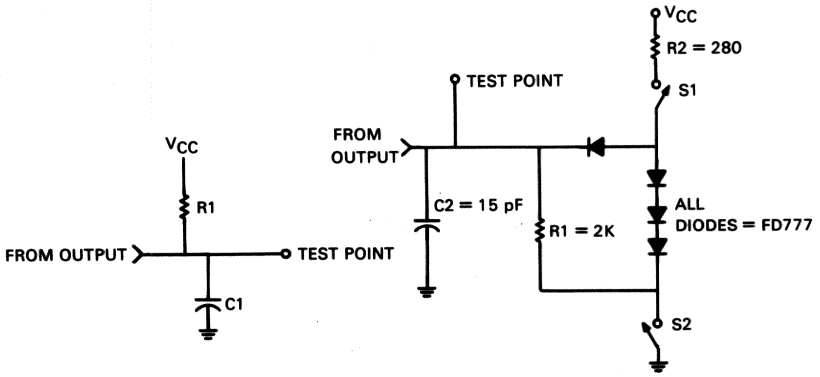

Figure 4 • DC005 Output Load Circuits

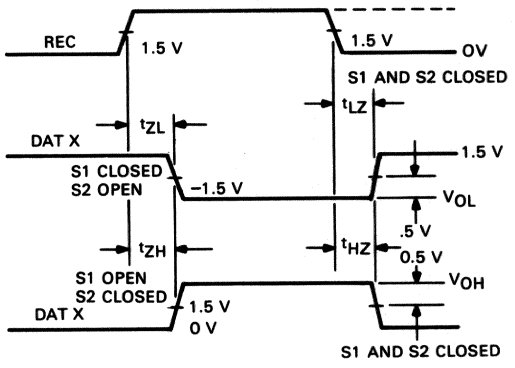

Figure 5 • DC005 Three-state Voltage Waveforms